



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/392,865	09/09/1999	SHOTA KITAMURA	005702-20035	1909

26021 7590 03/15/2002

HOGAN & HARTSON L.L.P.
500 S. GRAND AVENUE
SUITE 1900
LOS ANGELES, CA 90071-2611

EXAMINER

TRAN, THIEN F

ART UNIT	PAPER NUMBER
----------	--------------

2811

DATE MAILED: 03/15/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/392,865	KITAMURA ET AL.	
	Examiner	Art Unit	
	Thien F Tran	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 5-7, 16 and 17 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 5-7, 16 and 17 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____. | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Upon further consideration, the finality of the rejection of the last Office action is withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 16-17, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato (US 5,962,890) in view of Mori (JP 407161848).

Sato discloses a nonvolatile semiconductor memory device (Figs. 1-11) comprising a semiconductor substrate 105; memory transistors formed on said semiconductor substrate to perform nonvolatile storage of an electric charge in accordance with data, each of said memory transistors being an electrically rewritable memory transistor including a floating gate 103 formed over said semiconductor substrate via a first gate insulating film 111 and a control gate 102 formed over said floating gate via a second gate insulating film 114; an oxide film 115 formed on said substrate and at least on both sides of each said floating gate and both sides of each said control gate; and a wiring layer 101 formed over the gate stacks via an interlayer insulating film 113; and element separating regions 107 extending along one direction (see Fig. 8); and wherein groups of said memory transistors are arranged along said one direction and adjacent said element separating regions (see Fig. 2); in each of said

Art Unit: 2811

element separating regions, an element separating insulating film is formed on said substrate extending in said one direction; each of said floating gates is formed on each of said memory transistors between and to the exclusion of most of said element separating regions (see Fig. 3); said control gates extending in a direction perpendicular to said one direction and intersecting said memory transistors and said element separating regions, each said control gate being arranged on said element separating insulating films in said element separating regions. Sato does not disclose side walls of first silicon nitride film for protecting sides of said floating gate and said control gate of each said transistor, and an outer second silicon nitride film covering surfaces of said control gate, a source diffusion layer 109, a drain diffusion layer 110 and each of said side walls of each of said memory transistors. Sato does not disclose two oxide films, an oxide film and another oxide film formed between each said side wall and each of said floating and control gates, between each said side wall and said substrate, and only said another oxide film formed between each said side wall and each element separating insulating film. Mori discloses a nonvolatile semiconductor memory device (Fig. 2) comprising multi-layered insulating layers covering the gate stacks and the substrate, wherein an oxide film 29 formed by thermal oxidation on the sides of the floating gate 23 and the control gate 25 and the substrate, a nitride film 36, another oxide film 37 formed on a substrate and on both sides of each floating gate 23 and both sides of each control gate 25; side walls 30 of first silicon nitride film over said another oxide film; and a second silicon nitride film 41 covering surfaces of the control gate, a source diffusion layer, a drain diffusion layer and side walls 30. It would have been

Art Unit: 2811

obvious to a person having ordinary skill in the art at the time the invention was made to replace the oxide film 115 of Sato with the multi-layered insulating layers of Mori in order to inhibit loss of electrons from floating gate. Since said oxide film 29 is formed by thermal oxidation, said oxide film 29 is not formed on each element separating insulating film 107 since there is no available silicon atoms from the element separating insulating to react with oxygen to form silicon oxide film. As a result, only said another oxide film 37 is formed between each said side wall and each element separating insulating film 107, and the wiring layer 101 is formed over the second silicon nitride film 41 via an interlayer insulating film 113.

The claim limitation "formed by low-pressure CVD" is taken to be a product by process limitation and considered non-limiting. In a product-by-process claim, it is the patentability of the claimed product and not of the recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. Also, a product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al., 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by

Art Unit: 2811

a new method is not a patentable product, whether claimed in "product by process" claims or not.

Regarding claim 5, Sato discloses metal silicide films (102a, 109a, 110a) formed on the surfaces of said control gate, said source/drain diffusion layers of each of said transistors.

Regarding claim 6, Sato discloses said drain diffusion layer 110 connected to a bit line 101 via the metal silicide film 110a and the source diffusion layer 109 connected to a common source line 112 (Fig. 4) via the metal silicide film 112a respectively.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sato (US 5,962,890) in view of Mori (JP 407161848) as applied to claims 16-17, 5 and 6 above, and further in view of Santin et al. (US 5,907,171).

The modified Sato as described above does not explicitly disclose at least one of a low-voltage MOS transistor and a high-voltage MOS transistor formed as a peripheral circuit. It is conventional to form low-voltage transistor and high-voltage transistor as a peripheral circuit of a memory array to select and drive memory cells during circuit operations, as shown for example by Santin et al. Therefore, the incorporation of the conventional features into the modified Noda et al. would have been prima facie obvious.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

Art Unit: 2811

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien F Tran whose telephone number is (703) 308-4108. The examiner can normally be reached on 7:00AM - 3:30PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Application/Control Number: 09/392,865
Art Unit: 2811

Page 7

tt
March 13, 2002

Tom Thomas
TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800